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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/989,931 6861326
	Filing Date	November 21, 2001
	First Named Inventor	Gonzalez et al.
	Art Unit	2815
	Examiner Name	Jose R. Diaz
Total Number of Pages in This Submission	Attorney Docket Number	MI22-1801

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to a Technology Center (TC)
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<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	Additional Enclosures: Request for Certificate of Correction.	
	Patent No. 6,861,326 B2 Issued: March 1, 2005	
SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Individual	David G. Latwesen, Ph.D., Reg. No. 38,533 Wells St. John, P.S.	
Signature		
Date	5/22/06	

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No. 6,861,326 B2
Patent Issue Date March 1, 2005
Application Serial No. 09/989,931
Filing Date November 21, 2001
Assignee Micron Technology, Inc.
Inventorship Fernando Gonzalez et al.
Attorney's Docket No. MI22-1801
Title: Methods of Forming Semiconductor Circuitry

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. 1.322(a))

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Decision and Certificate of Correction
Branch of the Patent Issue Division

From: David G. Latwesen, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 6,861,326 B2, granted March 1, 2005, in accordance with the Certificate of Correction form attached hereto in duplicate.

The errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Since this Certificate of Correction is being requested due to PTO errors, it is believed that no fee is due. However, in the event that a fee is required for issuance of this Certificate of Correction, please charge the fee specified under 37 C.F.R. § 1.20(a) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

05/26/2006 EAREGAY2 00000005 230925 6861326


01 FC:1811 100.00 DA

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Attached hereto, in duplicate is Form PTO-1050, with at least one copy being suitable for printing.

Respectfully submitted,

Dated: 5/22/06

By: 
David G. Latwesen, Ph.D.
Reg. No. 38,533

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,861,326 B2
DATED : March 1, 2005
INVENTOR(S) : Gonzalez et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --4,903,108 2/1990 Young et al.
5,650,343 7/1997 Luning et al.--
Before "5,759,908".

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,306,691 B1 10/2001 Koh--
Before "6,358,806 B1".

Title Page, "References Cited", "U.S. PATENT DOCUMENTS",
Insert --6,566,210 B2 5/2003 Ajmera et al.--
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Insert --6,653,714 B2 11/2003 Matsuno et al.--
Before "2001/0008292 A1".

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Insert --OTHER PUBLICATIONS
Lee, W. et al., "Investigation of Poly-Si_{1-x}Ge_x for Dual-Gate CMOS Technology", IEEE
Electron Device Letters, Vol. 19, No. 7, July 1998, pp. 247-249.
Wolf, S., "Silicon Processing for the VLSI Era: Vol. 1: Process Technology", 1986
Lattice Press, pp. 191-195.
Before "** cited by examiner".

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1 of 1

Mailing Address of Sender:
David G. Latwesen, Ph.D.
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

Patent No. 6,861,326 B2

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Form PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-1801SERIAL NO.
09/989,931LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT:
Fernando Gonzalez et al.FILING DATE
Nov. 21, 2001 [RCE filed herewith]GROUP
2815

U.S. PATENT DOCUMENTS

Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
<i>2</i>	AA	6,653,714 B2	11/03	Matsuno et al.			
<i>2</i>	AB	4,903,108	02/90	Young et al.			
<i>2</i>	AC	6,566,210 B2	05/03	Ajmera et al.			
<i>2</i>	AD	5,650,343	07/97	Luning et al.			
<i>2</i>	AE	6,306,691 B1	10/01	Koh			
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AJ							
	AK							
	AL							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

<i>2</i>	AM	Lee, W. et al., "Investigation of Poly-Si ₃ Ge ₂ for Dual-Gate CMOS Technology", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp. 247-249.
<i>2</i>	AN	Wolf, S., "Silicon Processing for the VLSI Era: Vol. 1: Process Technology", 1986 Lattice Press, pp. 191-195.
	AO	

EXAMINER *[Signature]*

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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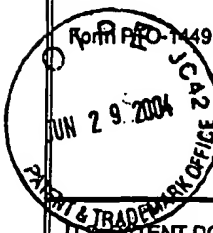
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